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IMPROVEMENT OF CARRIERS FOR SEMICONDUCTOR DEVICE TEST HANDLER USING AXIOMATIC DESIGN

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ABSTRACT

Apparatuses such as testers and test handlers are widely used together for test process of semiconductor devices. A carrier is a test handler component which carries a semiconductor device during test process. Some semiconductor devices are required to be tested at high temperature and low temperature as well as room temperature. The conventional carrier considerably deflects due to the test temperature variation. This causes unreliable results and frequent test handler jams.

To analyze the carrier design, functional requirements of carriers were defined: position the device on the socket, and let the carrier engage smoothly with the socket guide. Design parameters of the previous design adopting a pin-hole guidance mechanism are location of carrier holes, and diameter of the holes. The holes are on the diagonal opposite corners of the carrier, and deviate due to thermal deflection. It is analyzed that the design is coupled according to the independence axiom.

To overcome the thermal problem, new design parameters were found by changing the holes into slots and relocating them: location of carrier slots, and width of the slots. The two longitudinal slots restrict the carrier to vertical motion; the one lateral slot does the carrier to lateral motion. Although the slots deviate from their original positions due to thermal deflection, the device under test (DUT) at the center of the carrier does not move. The design becomes decoupled, and enables the concise design of carrier.

Keywords: Axiomatic Design, Handler, Carrier, Semiconductor

1 INTRODUCTION

Most of semiconductor device manufacturers have test processes for their own final products. To fill large mass production and urging delivery, the test processes have employed well-equipped and automated apparatuses such as testers and test handlers. A tester runs test programs and rates each semiconductor device. A test handler, which is almost always working with a tester, carries semiconductor devices and puts them on sockets during the program execution of the tester, and sorts them according to the test result sent from the tester.

Rapid strides of semiconductor technology brought about incredibly tiny semiconductor devices with the size of about 10×10 millimeters and more than one hundred leads on the face. The size is becoming smaller and the leads are more and finer. The distance between these leads measures around 0.8 millimeters and the size of leads 0.4 millimeters or less.

Semiconductor devices are tested by electric current which flows through contacts between each device lead and socket lead. In order to obtain more reliable test results, the sufficient contact pressure and contact area should be guaranteed because electric resistance at the contact point rises under the inadequate contact condition. Deviation of about 0.1 millimeters may be significant for the contact area and bring about unreliable results. Therefore, positioning the device is one of the most important tasks for the test reliability.

A test tray is a frame which has 64 to 256 carriers in array, and each carrier holds and carries a semiconductor device during the test. Semiconductor devices are required to be tested at high temperature of 80 to 120 degrees of Celsius and low temperature of -5 to -30 as well as room temperature. A test tray is heated (or frozen) in the hot (or cold) chamber and moved to the test chamber. In the test chamber, the test tray confronts the array of sockets on the handler-tester interface (HTI). The press module pushes each carrier so that each carrier engages with the corresponding socket. While the test program is running, the press module maintains its pressing load. After the testing job, the pressing load is released and the carriers turn back to the normal position in the test tray. Finally, the test tray transfers to the cooling (or defrosting) chamber and then is reloaded in the pick-and-place (sorting) section.

2 CONVENTIONAL CARRIER

A pin-hole guidance mechanism has been adopted for the carrier-socket engagement. Strictly speaking, the socket is set in the middle of the socket guide, and the socket guide practically engages with the carrier so that the device can contact with the socket. The carrier has two guide holes on the diagonal opposite

corners, and the socket guide also has two corresponding guide pins so that each pin can insert into the hole. The carrier and the socket guide are shown in Figure 1.

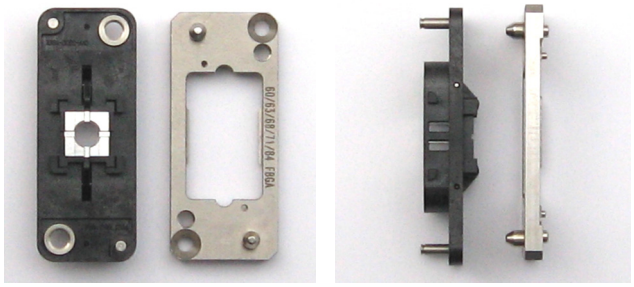

Figure 1 – Conventional carrier and socket guide.

This guidance mechanism has a serious problem caused by thermal deflection. Clearance between a hole and a pin should be small enough since each device has to be positioned within 0.1 millimeters tolerance. Contradictorily, the clearance should be large enough at the same time because the carrier will be tightly stuck if the hole deviates too much from its original position due to thermal expansion or contraction during the hot or cold test. This causes unreliable test results and frequent test handler jams. Furthermore, the carriers are made of polyether imide (PEI) resin, which expands considerably large comparing with other metallic materials of which the socket guides are made.

To design the carrier, functional requirements are defined, which are listed in Table 1.

FR_1		**Position the device precisely on the socket.**
FR_{11}	δ_x	Limit the deviation of lateral position to under 0.1 mm.
FR_{12}	δ_y	Limit the deviation of longitudinal position to under 0.1 mm.
FR_2		**Let the carrier engage smoothly with the socket guide.**
FR_{21}	ε_x	Maintain the lateral clearance between a pin and a hole.
FR_{22}	ε_y	Maintain the longitudinal clearance between a pin and a hole.

Table 1 – Functional requirements of the conventional carrier design.

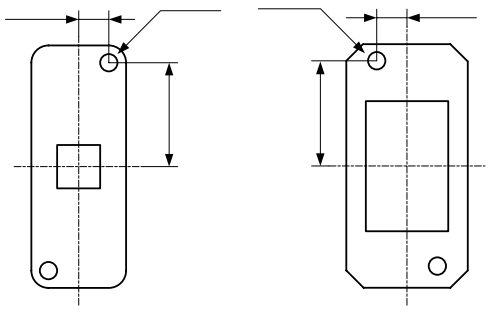

Figure 2 –Schematic of the conventional carrier and socket guide.

The deviation of the device position and the clearance can be described by position of the hole, position of the pin, diameter of the hole, diameter of the pin and the thermal expansion coefficient.

Considering the lateral direction, the device position is limited under each condition of following two cases.

Mode 1: $X_{\text{hole}}\left(1+\alpha\left(T-T_{\text{room}}\right)\right) \geq X_{\text{pin}}$

The deviation of lateral position δ_x is constrained by

$$\delta_{x,\max} = \left(X_{\text{pin}} - \frac{D_{\text{pin}}}{2}\right) - \left(X_{\text{hole}} + X_{\text{hole}}\alpha\left(T-T_{\text{room}}\right) - \frac{D_{\text{hole}}}{2}\right) \leq 0.1$$

and

$$\delta_{x,\min} = \left(-X_{\text{pin}} + \frac{D_{\text{pin}}}{2}\right) - \left(-X_{\text{hole}} - X_{\text{hole}}\alpha\left(T-T_{\text{room}}\right) + \frac{D_{\text{hole}}}{2}\right) \geq -0.1$$

Combining these two relations, the deviation of lateral position can be obtained as

$$\delta_x = \frac{D_{\text{hole}} - D_{\text{pin}}}{2} - \left[X_{\text{hole}}\left(1+\alpha\left(T-T_{\text{room}}\right)\right) - X_{\text{pin}}\right] \leq 0.1 \qquad (1)$$

The lateral clearance ε_x is defined as

$$\varepsilon_x = \frac{D_{\text{hole}} - D_{\text{pin}}}{2} - \left[X_{\text{hole}}\left(1+\alpha\left(T-T_{\text{room}}\right)\right) - X_{\text{pin}}\right] \geq 0 \qquad (2)$$

Mode 2: $X_{\text{hole}}\left(1+\alpha\left(T-T_{\text{room}}\right)\right) \leq X_{\text{pin}}$

Similarly, the deviation of lateral position and the lateral clearance are

$$\delta_x = \frac{D_{\text{hole}} - D_{\text{pin}}}{2} - \left[X_{\text{pin}} - X_{\text{hole}}\left(1+\alpha\left(T-T_{\text{room}}\right)\right)\right] \leq 0.1 \qquad (3)$$

and

$$\varepsilon_x = \frac{D_{\text{hole}} - D_{\text{pin}}}{2} - \left[X_{\text{pin}} - X_{\text{hole}}\left(1+\alpha\left(T-T_{\text{room}}\right)\right)\right] \geq 0 \qquad (4)$$

Following the same procedure as the lateral direction case, it is easy to show that the deviation of longitudinal position and the longitudinal clearance can be written as

$$\delta_y = \frac{D_{\text{hole}} - D_{\text{pin}}}{2} - \left[Y_{\text{hole}}\left(1+\alpha\left(T-T_{\text{room}}\right)\right) - Y_{\text{pin}}\right] \leq 0.1 \qquad (5)$$

and

$$\varepsilon_y = \frac{D_{\text{hole}} - D_{\text{pin}}}{2} - \left[Y_{\text{hole}} \left(1 + \alpha \left(T - T_{\text{room}}\right)\right) - Y_{\text{pin}} \right] \geq 0 \qquad (6)$$

for Mode 1, and

$$\delta_y = \frac{D_{\text{hole}} - D_{\text{pin}}}{2} - \left[Y_{\text{pin}} - Y_{\text{hole}} \left(1 + \alpha \left(T - T_{\text{room}}\right)\right) \right] \leq 0.1 \qquad (7)$$

and

$$\varepsilon_y = \frac{D_{\text{hole}} - D_{\text{pin}}}{2} - \left[Y_{\text{pin}} - Y_{\text{hole}} \left(1 + \alpha \left(T - T_{\text{room}}\right)\right) \right] \geq 0 \qquad (8)$$

for Mode 2.

Because the dimensions of the pin and test temperature are previously determined, δ_x, δ_y, ε_x and ε_y are related to only the dimensions of the hole and the thermal expansion coefficient of the carrier material. Therefore, the design parameters are chosen as Table 2.

DP_1	**Position of the hole**	
DP_{11}	X_{hole}	Lateral position of the hole
DP_{12}	Y_{hole}	Longitudinal position of the hole
DP_{13}	α	Thermal expansion coefficient of the carrier material
DP_2	**Diameter of the hole**	
DP_{21}	D_{hole}	Diameter of hole

Table 2 – Design parameters of the conventional carrier design.

For all the cases, the design equation is derived as

$$\begin{bmatrix} \delta_x \\ \delta_y \\ \varepsilon_x \\ \varepsilon_y \end{bmatrix} = \begin{bmatrix} A_{11} & 0 & A_{13} & A_{14} \\ 0 & A_{22} & A_{23} & A_{24} \\ A_{31} & 0 & A_{33} & A_{34} \\ 0 & A_{42} & A_{43} & A_{44} \end{bmatrix} \begin{bmatrix} X_{\text{hole}} \\ Y_{\text{hole}} \\ \alpha \\ D_{\text{hole}} \end{bmatrix} \qquad (9)$$

From the design matrix of Equation (9), it is found that the conventional carrier design is highly coupled according to the independence axiom.

3 NEW CARRIER

A new carrier design is proposed adopting a pin-slot guidance mechanism to overcome the thermal problem.

In Equation (9), all the functional requirements rely on the thermal expansion coefficient and the hole diameter. This implies that the coupled design can be improved by separating the effect of the thermal expansion and the hole into each independent direction. Changing the holes into slots and relocating the slots and the pins, the thermal deflection and directional dependency can be excluded indeed.

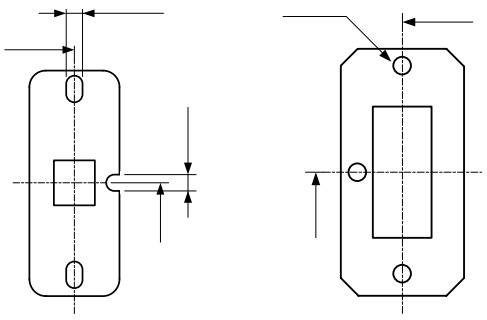

Figure 3 –Schematic of the new carrier and socket guide.

The deviation of position and clearance of each direction are

$$\delta_x = \left(X_{\text{pin}} - X_{\text{slot}}\right) + \frac{W_{\text{slot},x} - D_{\text{pin}}}{2} \leq 0.1 \qquad (10)$$

$$\delta_x = \left(X_{\text{pin}} - X_{\text{slot}}\right) - \frac{W_{\text{slot},x} - D_{\text{pin}}}{2} \geq -0.1 \qquad (11)$$

$$\varepsilon_x = W_{\text{slot},x} - D_{\text{pin}} \geq 0 \qquad (12)$$

for the lateral direction, and

$$\delta_y = \left(Y_{\text{pin}} - Y_{\text{slot}}\right) + \frac{W_{\text{slot},y} - D_{\text{pin}}}{2} \leq 0.1 \qquad (13)$$

$$\delta_y = \left(Y_{\text{pin}} - Y_{\text{slot}}\right) - \frac{W_{\text{slot,y}} - D_{\text{pin}}}{2} \geq -0.1 \qquad (14)$$

$$\varepsilon_y = W_{\text{slot},y} - D_{\text{pin}} \geq 0 \qquad (15)$$

for the longitudinal direction. No thermal expansion term is contained in these relations, which means the thermal effect is completely excluded.

From these relations, new design parameters are found, which are listed in Table 3.

DP_1	**Position of the slot**	
DP_{11}	X_{slot}	Lateral position of the longitudinal slot
DP_{12}	Y_{slot}	Longitudinal position of the lateral slot
DP_2	**Width of the slot**	
DP_{21}	$W_{slot,x}$	Width of the lateral slot
DP_{22}	$W_{slot,y}$	Width of the longitudinal slot

Table 3 – Design parameters of the new carrier design.

Therefore, the design equation of the new carrier design becomes

$$\begin{bmatrix} \delta_x \\ \delta_y \\ \varepsilon_x \\ \varepsilon_y \end{bmatrix} = \begin{bmatrix} A_{11} & 0 & A_{13} & 0 \\ 0 & A_{22} & 0 & A_{24} \\ 0 & 0 & A_{33} & 0 \\ 0 & 0 & 0 & A_{44} \end{bmatrix} \begin{bmatrix} X_{slot} \\ Y_{slot} \\ W_{slot,x} \\ W_{slot,y} \end{bmatrix} \quad (16)$$

which is said a decoupled design.

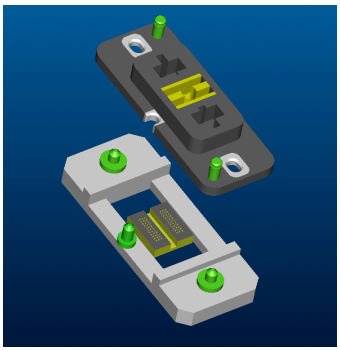

Figure 4 – New carrier and socket guide design.

4 CONCLUSIONS

It is analyzed that the conventional carrier with the pin-hole guidance mechanism is highly coupled.

A new carrier is proposed by changing the holes into the slots and relocating the slots and the pins, which decouples the design and excludes the thermal deflection. Consequently, use of such carriers with the pin-slot guidance mechanism should enable the concise design of carriers and lower the cost of the test handler operation.

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